IN THE CLAIMS

Please cancel without prejudice claims 22 and 24.

Please amend claims 1-9 as indicated below.

---

1. (Currently Amended) A system comprising:

a processor; and

a memory device coupled to the processor and contained within a single integrated circuit, the memory device including:

a main memory; ~~and~~

a cache memory coupled to the processor and to the main memory to ~~simultaneously contain multiple addresses representing data requested from the main memory~~ stored recently accessed data and addresses associated with the recently accessed data; and

a wait control logic coupled to the processor, the main memory, and the cache memory, the wait control logic signaling the processor, if data currently requested is not in the cache memory, to indicate that the requested data is not ready to be read, and the wait control logic signaling the processor to indicate that the requested data is ready to be read on a next processor cycle, if the requested data is in the cache memory.

C1

2. (Currently Amended) The system of claim 1, wherein the memory device further comprises an address latch logic to receive the addresses of the requested data, and wherein the cache memory of the memory device further comprises:

an address cache memory coupled to the address latch logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched; and

a data cache memory coupled to the address cache memory and the main memory to store the recently accessed data, the data cache memory receiving data from the main memory if the data requested is not in the data cache memory.

~~wherein: all circuitry to operate the cache memory is contained within the memory device.~~

C1

3. (Currently Amended) The system of claim [[1]] 2, wherein the memory device further comprises a comparator coupled to the address latch logic and the address cache memory, an output of the comparator coupling to the wait control logic to cause the wait control logic to assert ~~asserting~~ the signal to the processor if the address stored in the address latch logic is not found in the address cache memory.

~~wherein: the main memory is a flash memory.~~

4. (Currently Amended) The system of claim [[1]] 3, wherein the comparator causes the wait control logic to assert a signal having one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory.

~~wherein: the cache memory can hold no more than sixteen addresses at the same time.~~

5. (Currently Amended) The system of claim [[1]] 2, wherein the address of the requested data is not presented to the main memory if the address of the requested data is found in the address cache memory.

~~wherein: the processor is contained within the single integrated circuit.~~

6. (Currently Amended) An apparatus comprising:

a memory device ~~to couple~~ capable of coupling to a processor through a bus, the memory device including on a single integrated circuit:

a main memory; ~~and~~

a cache memory coupled to the main memory stored recently accessed data and addresses associated with the recently accessed data; and ~~to store data in adjacent locations in the cache memory from non-consecutive addresses requested from the main memory.~~

a wait control logic coupled to the main memory and the cache memory, the wait control logic capable of signaling the processor through the bus, if data currently requested is not in the cache memory, to indicate that the requested data is not ready to be read, and the wait control logic capable of signaling the processor to indicate that the requested data is ready to be read on a next processor cycle, if the requested data is in the cache memory.

7. (Currently Amended) The apparatus of claim 6, wherein the memory device further comprises an address latch logic to receive the addresses of the requested data, and wherein the cache memory of the memory device further comprises:

an address cache memory coupled to the address latch logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched; and

a data cache memory coupled to the address cache memory and the main memory to store the recently accessed data, the data cache memory receiving data from the main memory if the data requested is not in the data cache memory.

~~wherein: all circuitry to operate the cache memory is contained within the memory device.~~

8. (Currently Amended) The apparatus of claim [[6]] 7, wherein the memory device further comprises a comparator coupled to the address latch logic and the address cache memory, an output of the comparator coupling to the wait control logic to cause the wait control logic asserting to assert the signal to the processor if the address stored in the address latch logic is not found in the address cache memory.

~~wherein: the main memory is a flash memory.~~

C1

9. (Currently Amended) The apparatus of claim [[6]] 8, wherein the comparator causes the wait control logic to assert a signal having one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory.

~~wherein: the cache memory can hold no more than sixteen addresses at the same time.~~

10-20. (Cancelled)

21. (Previously Presented) The system of claim 1, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

22. (Cancelled)

23. (Previously Presented) The apparatus of claim 6, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

24. (Cancelled)